



Description

JMT N And P-Channel Enhancement Mode MOSFET

Features

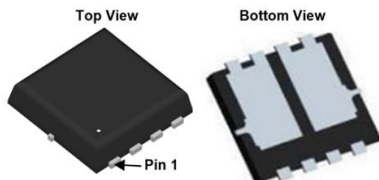
- N-Channel: 30V, 10A
 $R_{DS(ON)} < 18m\Omega @ V_{GS} = 10V$
 $R_{DS(ON)} < 28m\Omega @ V_{GS} = 4.5V$
- P-Channel: -30V, -8A
 $R_{DS(ON)} < 31m\Omega @ V_{GS} = -10V$
 $R_{DS(ON)} < 49m\Omega @ V_{GS} = -4.5V$
- Excellent Gate Charge x $R_{DS(ON)}$ Product(FOM)
- Very Low On-resistance $R_{DS(ON)}$
- Fast Switching Speed

Application

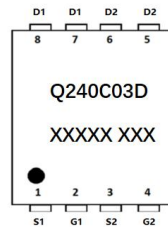
- Battery Protection
- Load Switch
- Power Management



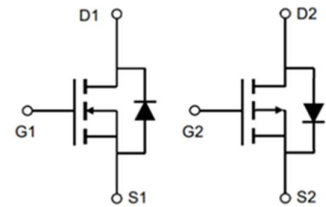
100% UIS TESTED!
100% ΔVds TESTED!



PDFN3x3-8L-D



Marking and pin Assignment



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	OUTLINE	Device Package	Reel Size	Reel (PCS)	Per Carton (PCS)
Q240C03D	JMTQ240C03D	TAPING	PDFN3x3-8L-D	13inch	5000	50000

Absolute Maximum Ratings (T_C=25°C unless otherwise specified)

Symbol	Parameter	Max. N-Channel	Max. P-Channel	Units
V _{DSS}	Drain-Source Voltage	30	-30	V
V _{GSS}	Gate-Source Voltage	±20	±20	V
I _D	Continuous Drain Current	T _C = 25°C	-8	A
		T _C = 100°C	-5.2	A
I _{DM}	Pulsed Drain Current ^{note1}	40	-32	A
E _{AS}	Single Pulsed Avalanche Energy ^{note2}	11	23	mJ
P _D	Power Dissipation	T _C = 25°C	3.4	W
R _{θJA}	Thermal Resistance, Junction to Ambient	40	37	°C/W
T _J , T _{STG}	Operating and Storage Temperature Range	-55 to +150		°C



N-Channel Electrical Characteristics (T_J=25°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristic						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	30	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =30V, V _{GS} =0V	-	-	1	μA
I _{GSS}	Gate to Body Leakage Current	V _{DS} =0V, V _{GS} =±20V	-	-	±100	nA
On Characteristics						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1.0	1.5	2.5	V
R _{DS(on)}	Static Drain-Source on-Resistance <small>note2</small>	V _{GS} =10V, I _D =5A	-	14	18	mΩ
		V _{GS} =4.5V, I _D =3A	-	20	28	mΩ
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{DS} =15V, V _{GS} =0V, f=1.0MHz	-	490	-	pF
C _{oss}	Output Capacitance		-	79	-	pF
C _{rss}	Reverse Transfer Capacitance		-	61	-	pF
Q _g	Total Gate Charge	V _{DS} =15V, I _D =5A, V _{GS} =10V	-	5.2	-	nC
Q _{gs}	Gate-Source Charge		-	0.9	-	nC
Q _{gd}	Gate-Drain("Miller") Charge		-	1.3	-	nC
Switching Characteristics						
t _{d(on)}	Turn-on Delay Time	V _{DS} =15V, I _D =3A, V _{GS} =10V, R _{REN} =3Ω	-	4.5	-	ns
t _r	Turn-on Rise Time		-	2.5	-	ns
t _{d(off)}	Turn-off Delay Time		-	14.5	-	ns
t _f	Turn-off Fall Time		-	3.5	-	ns
Drain-Source Diode Characteristics and Maximum Ratings						
I _S	Maximum Continuous Drain to Source Diode Forward Current		-	-	10	A
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	40	A
V _{SD}	Drain to Source Diode Forward Voltage	V _{GS} =0V, I _S =10A	-	0.8	1.2	V

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. EAS condition : T_J=25°C, V_{DD}=15V, V_G=10V, L=0.5mH, R_g=25Ω, I_{AS}=6.5A

3. Pulse Test: Pulse Width≤300μs, Duty Cycle≤0.5%



P-Channel Electrical Characteristics (T_J=25°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristic						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D = -250μA	-30	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = -30V, V _{GS} =0V,	-	-	-1	μA
I _{GSS}	Gate to Body Leakage Current	V _{DS} =0V, V _{GS} = ±20V	-	-	±100	nA
On Characteristics						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D = -250μA	-1.0	-1.6	-2.5	V
R _{DS(on)}	Static Drain-Source on-Resistance <small>note3</small>	V _{GS} = -10V, I _D = -7A	-	24	31	mΩ
		V _{GS} = -4.5V, I _D = -4A	-	35	49	
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{DS} = -15V, V _{GS} =0V, f=1.0MHz	-	982	-	pF
C _{oss}	Output Capacitance		-	135	-	pF
C _{rss}	Reverse Transfer Capacitance		-	109	-	pF
Q _g	Total Gate Charge	V _{DS} = -15V, I _D = -4A, V _{GS} = -10V	-	10	-	nC
Q _{gs}	Gate-Source Charge		-	2	-	nC
Q _{gd}	Gate-Drain("Miller") Charge		-	2.7	-	nC
Switching Characteristics						
t _{d(on)}	Turn-on Delay Time	V _{DD} = -15V, I _D = -7A, V _{GS} = -10V, R _{GEN} =2.5Ω	-	11	-	ns
t _r	Turn-on Rise Time		-	19	-	ns
t _{d(off)}	Turn-off Delay Time		-	45	-	ns
t _f	Turn-off Fall Time		-	26	-	ns
Drain-Source Diode Characteristics and Maximum Ratings						
I _S	Maximum Continuous Drain to Source Diode Forward Current		-	-	-8	A
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	-32	A
V _{SD}	Drain to Source Diode Forward Voltage	V _{GS} =0V, I _S = -8A	-	-0.8	-1.2	V

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. EAS condition : T_J=25°C, V_{DD}= -15V, V_G= -10V, L=0.5mH, R_g=25Ω, I_{AS}= -9.5A

3. Pulse Test: Pulse Width≤300μs, Duty Cycle≤0.5%



Typical Performance Characteristics-N

Figure 1: Output Characteristics

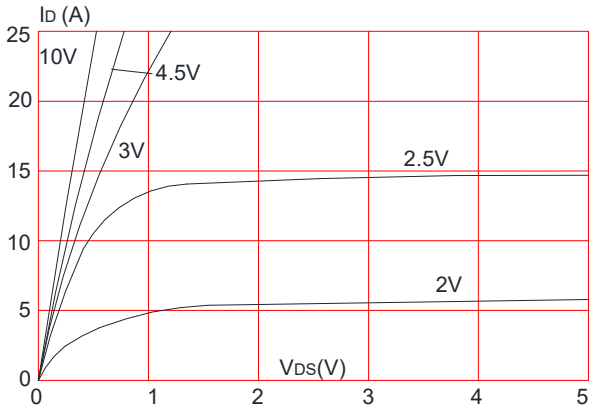


Figure 2: Typical Transfer Characteristics

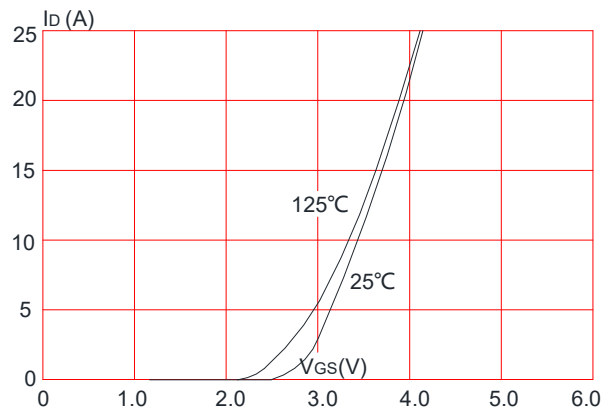


Figure 3: On-resistance vs. Drain Current

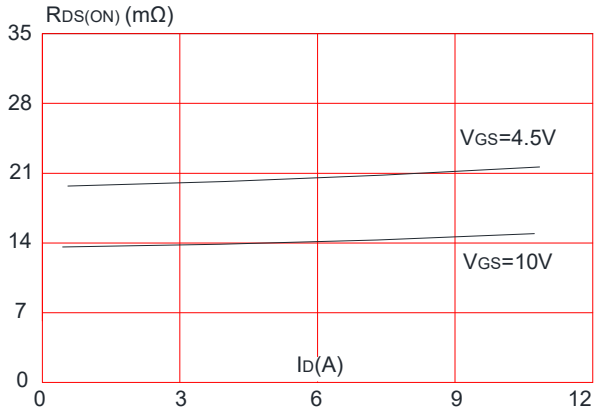


Figure 4: Body Diode Characteristics

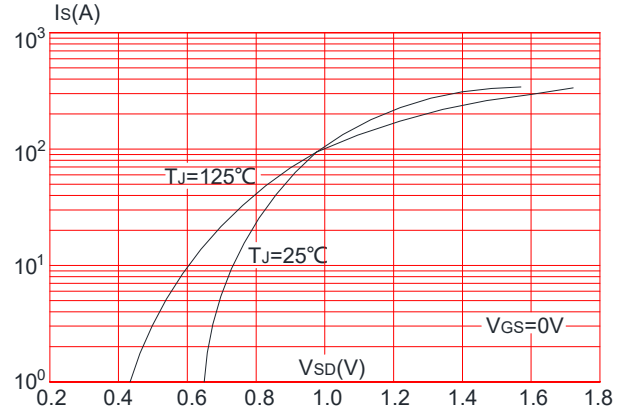


Figure 5: Gate Charge Characteristics

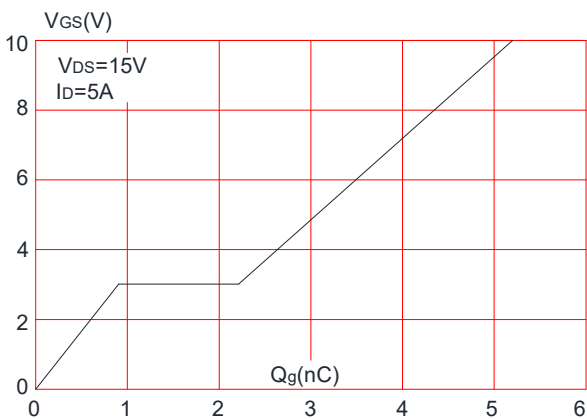


Figure 6: Capacitance Characteristics

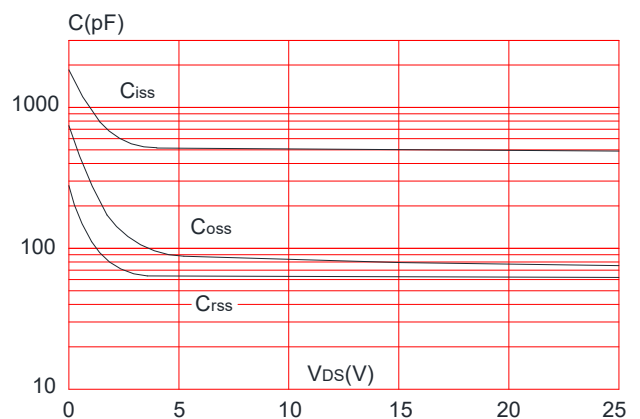




Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

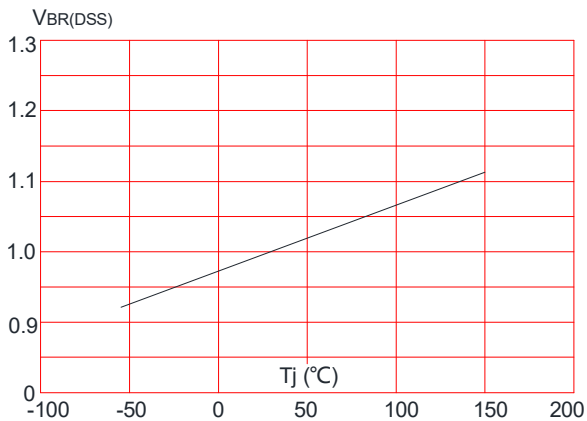


Figure 8: Normalized on Resistance vs. Junction Temperature

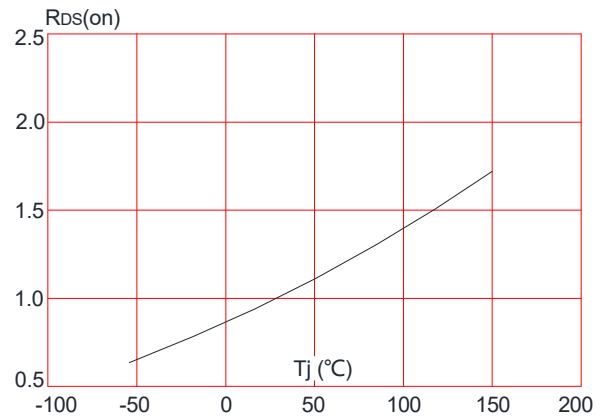


Figure 9: Maximum Safe Operating Area

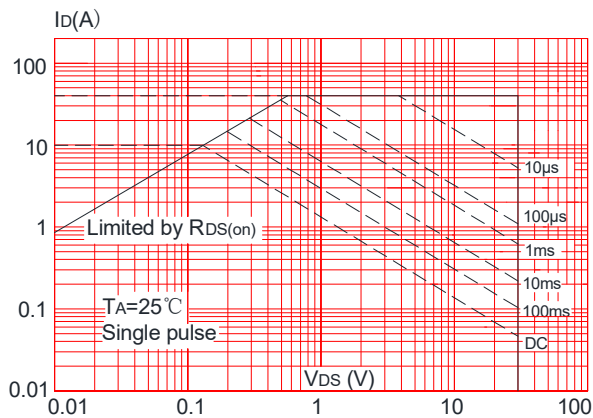


Figure 10: Maximum Continuous Drain Current vs. Ambient Temperature

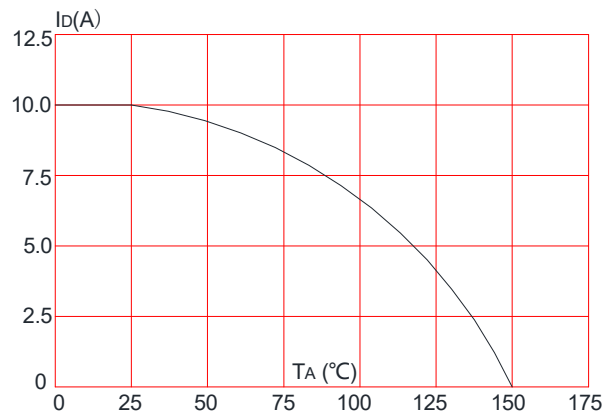
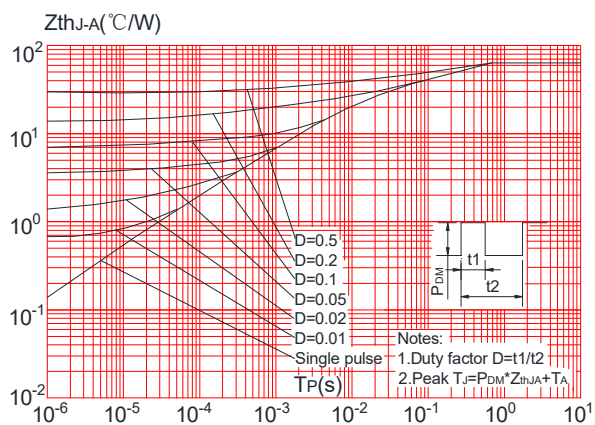


Figure 11: Maximum Effective Transient Thermal Impedance, Junction-to-Ambient



Test Circuit-N

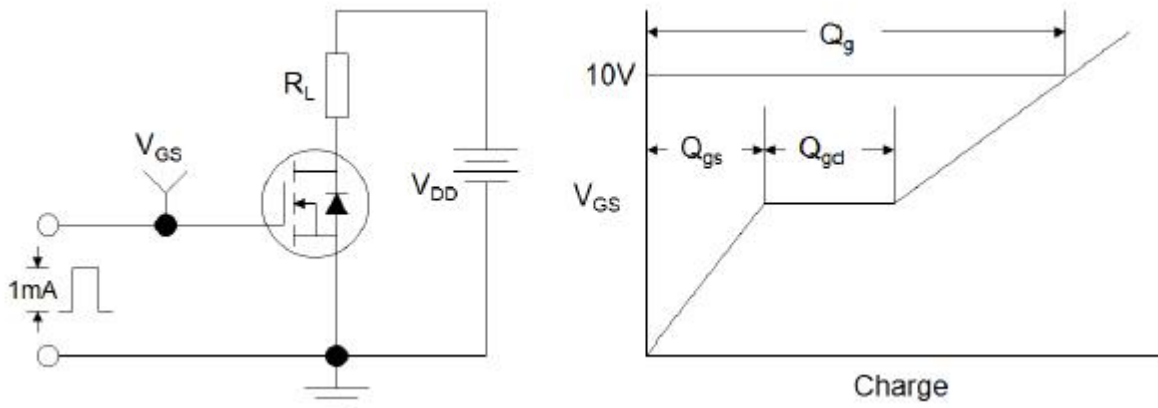


Figure1:Gate Charge Test Circuit & Waveform

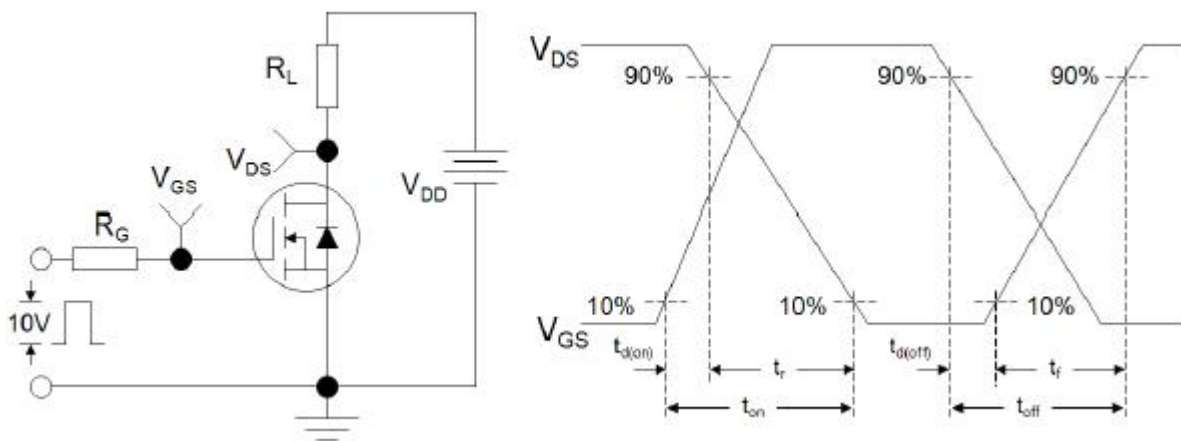


Figure 2: Resistive Switching Test Circuit & Waveforms

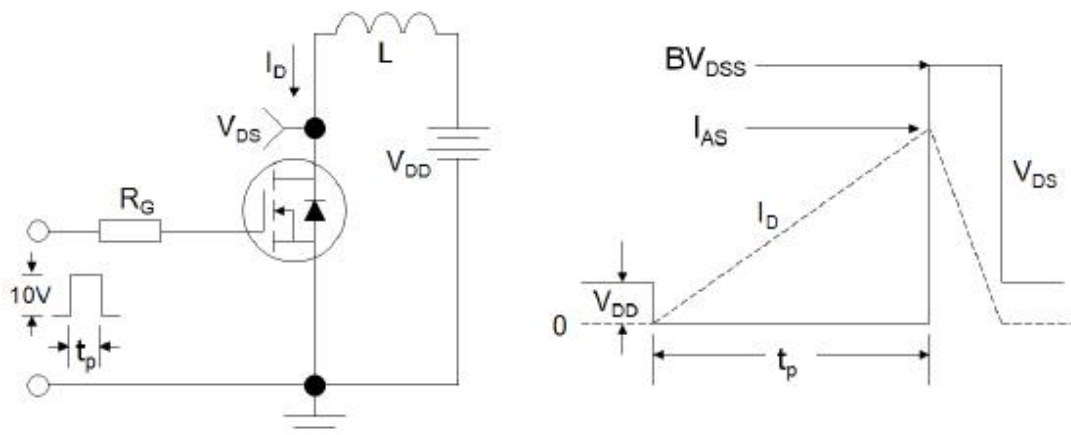


Figure 3:Unclamped Inductive Switching Test Circuit & Waveforms



Typical Performance Characteristics-P

Figure 1: Output Characteristics

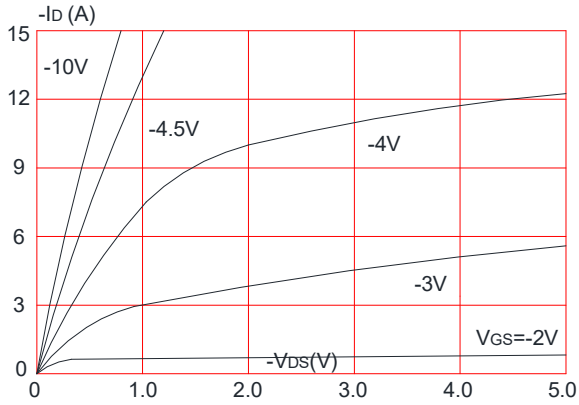


Figure 2: Typical Transfer Characteristics

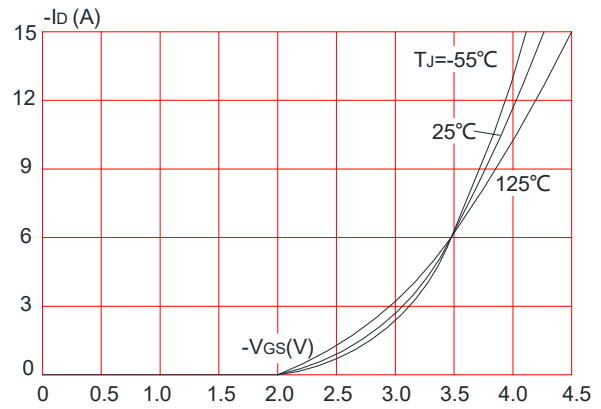


Figure 3: On-resistance vs. Drain Current

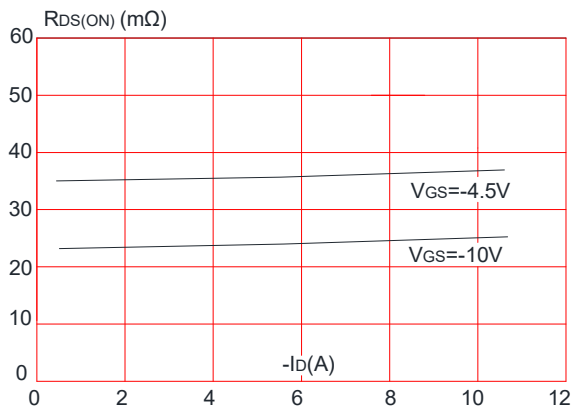


Figure 4: Body Diode Characteristics

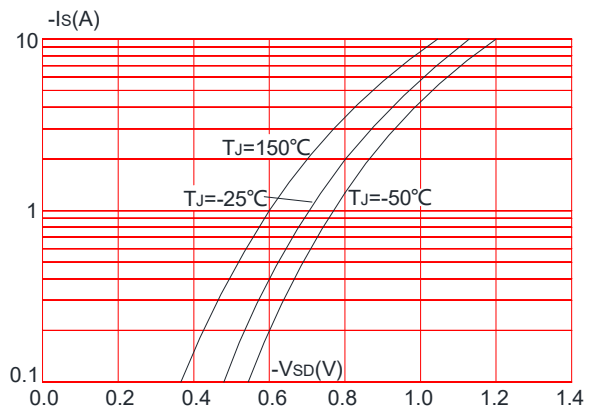


Figure 5: Gate Charge Characteristics

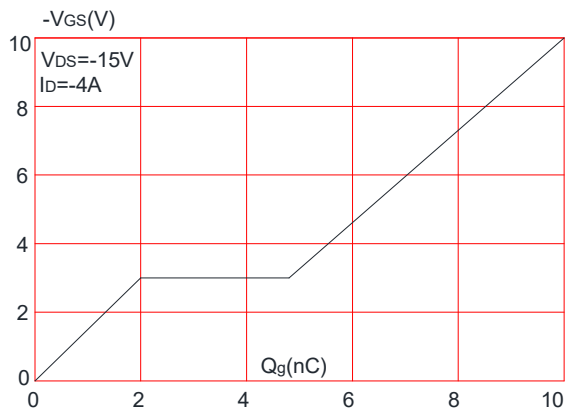


Figure 6: Capacitance Characteristics

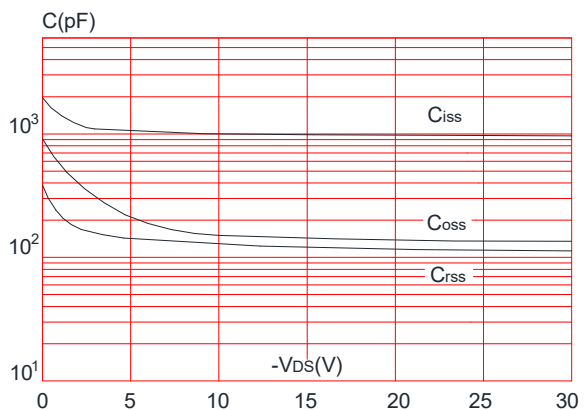




Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

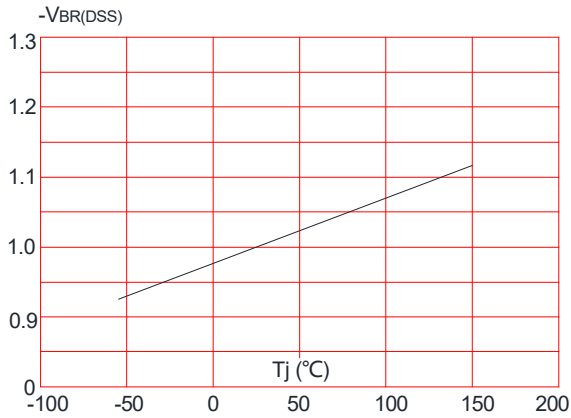


Figure 8: Normalized on Resistance vs. Junction Temperature

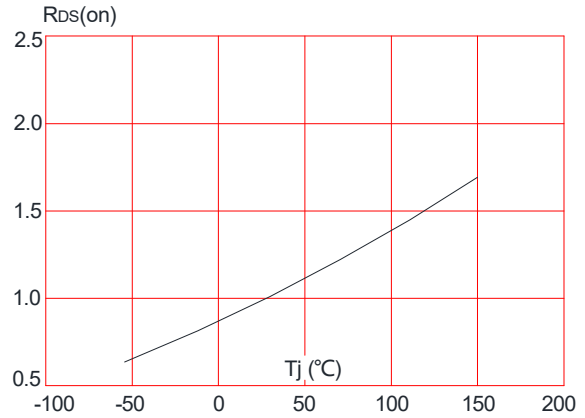


Figure 9: Maximum Safe Operating Area

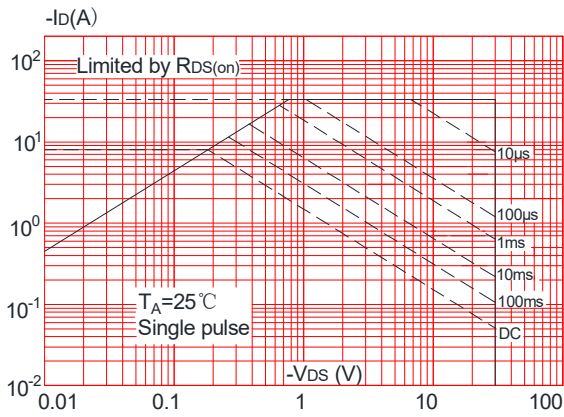


Figure 10: Maximum Continuous Drain Current vs. Case Temperature

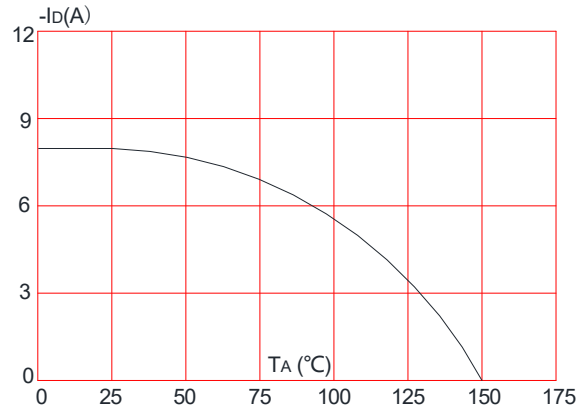
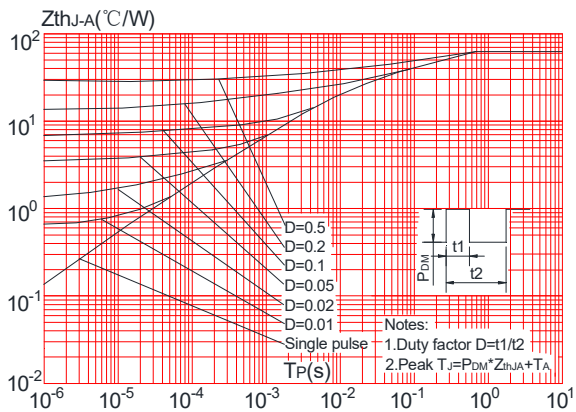
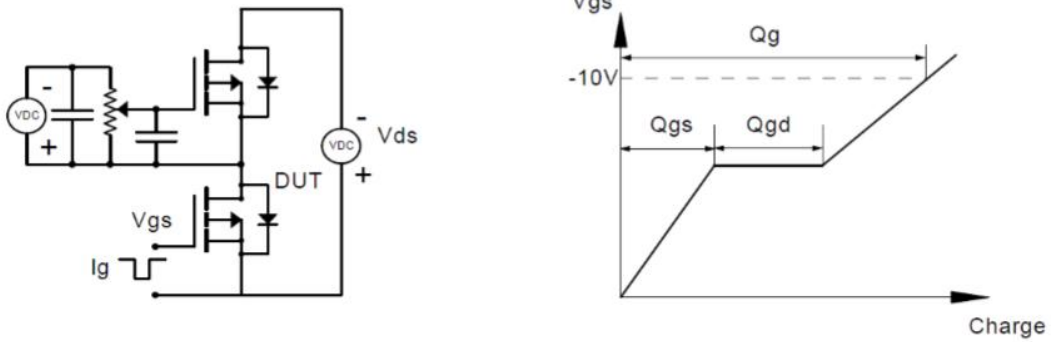


Figure 11: Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

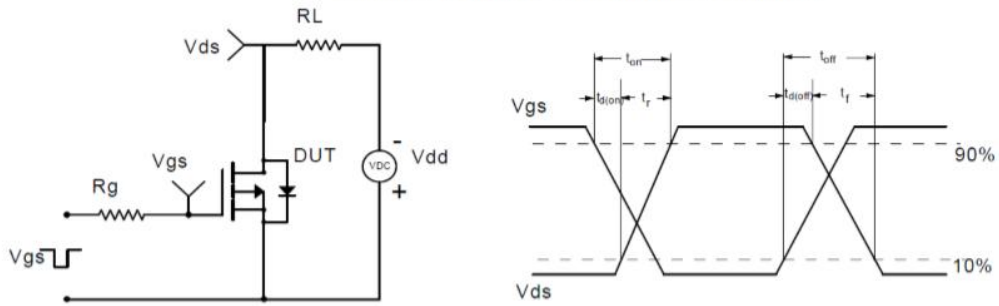


Test Circuit-P

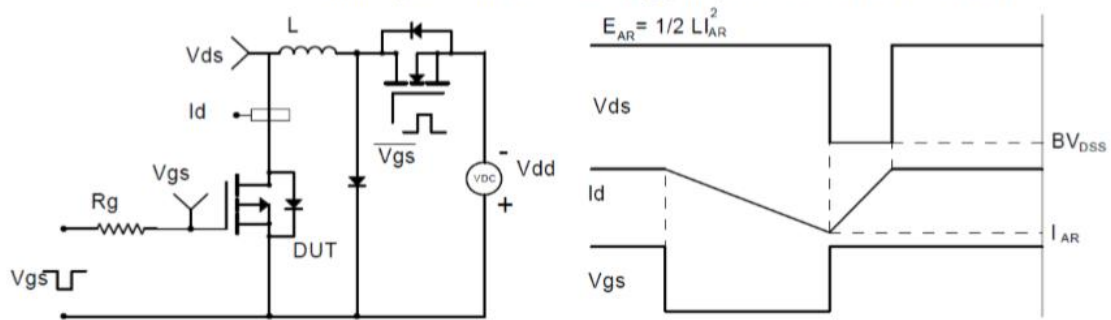
Gate Charge Test Circuit & Waveform



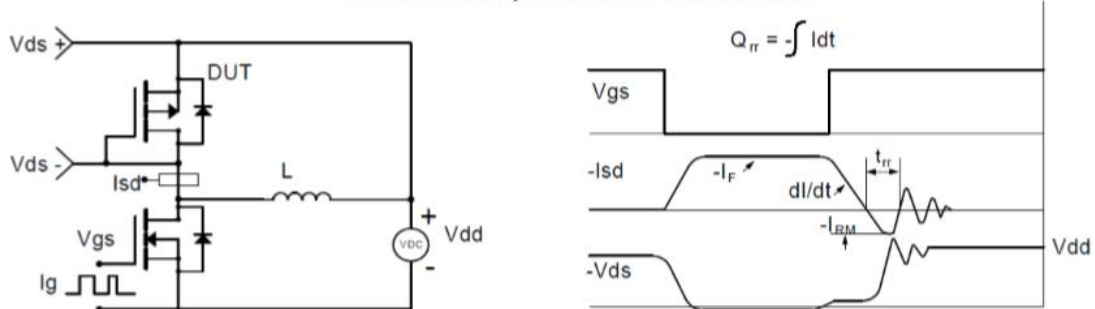
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

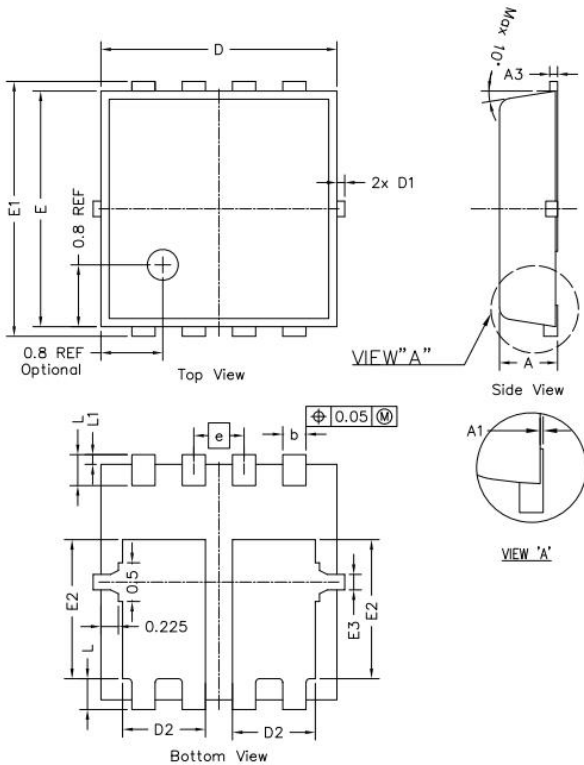


Diode Recovery Test Circuit & Waveforms





Package Mechanical Data-PDFN3x3-8L-D



SYMBOLS	DIMENSION IN MM			DIMENSION IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.700	0.750	0.800	0.028	0.030	0.031
A1	---	---	0.050	----	----	0.002
A3	0.144	0.152	0.202	0.006	0.006	0.008
b	0.250	0.300	0.350	0.010	0.012	0.014
e	0.65 BSC			0.026 BSC		
D	2.950	3.050	3.150	0.116	0.120	0.124
E	2.950	3.050	3.150	0.116	0.120	0.124
D1	---	---	0.125	----	----	0.005
E1	3.200	3.300	3.400	0.126	0.130	0.134
D2	0.970	1.070	1.170	0.038	0.042	0.046
E2	1.700	1.800	1.900	0.067	0.071	0.075
E3	0.150	0.200	0.250	0.006	0.008	0.010
L	0.300	0.400	0.500	0.012	0.016	0.020
L1	0.075	0.125	0.175	0.003	0.005	0.007

Information furnished in this document is believed to be accurate and reliable. However, Jiangsu JieJie Microelectronics Co.,Ltd assumes no responsibility for the consequences of use without consideration for such information nor use beyond it.

Information mentioned in this document is subject to change without notice, apart from that when an agreement is signed, Jiangsu JieJie complies with the agreement.

Products and information provided in this document have no infringement of patents. Jiangsu JieJie assumes no responsibility for any infringement of other rights of third parties which may result from the use of such products and information.



is a registered trademark of Jiangsu JieJie Microelectronics Co.,Ltd.

Copyright ©2022 Jiangsu JieJie Microelectronics Co.,Ltd. Printed All rights reserved.